Chun-Kai Chang

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https://chunkaichang.com

Ph.D. in computer architecture

EXPERIENCE

Intel Corporation — Software Engineering Intern
05/2019 - 08/2019 | Aloha, OR
Developed near-storage computing with 1.5X speedup and
Virtualized hybrid storage as a service for low cost and high performance

Hewlett Packard Enterprise — Research Intern
05/2017 - 08/2017 | Palo Alto, CA
Created a performance model for multi-GPU clusters with >90% accuracy

The University of Texas at Austin — Research Assistant
06/2016 - 05/2019 | Austin, TX
Published 7 papers on system reliability (2 top-tier conference papers)

The University of Texas at Austin — Teaching Assistant
08/2019 - 12/2019 and 09/2015 - 06/2016 | Austin, TX
Taught Computer Architecture and Introduction to Embedded Systems

EDUCATION

The University of Texas at Austin — ECE Ph.D.
08/2015 - 05/2020 | Austin, TX | GPA: 3.80
Dissertation: High-Fidelity Error Injection and Acceleration Techniques

National Chiao Tung University — EECS B.S.
08/2010 - 06/2014 | Hsinchu, Taiwan | GPA: 3.99

PROJECTS

Hamartia: An Open-Source† Error Injection and Detection Suite
Evaluated the impact of random hardware errors at the gate level, the micro-architectural level, and the ISA level | C++, Python, and Verilog

Scan-Resistant Replacement Policies for Multi-Core LLC
Studied last-level cache replacement policies on a quad-core ARM system and achieved 9% average speedup over LRU | C++, gem5

Emulating A Computer System Using Queuing Networks
Modeled performance of a computer (including CPU, memory, disks, Ethernet, and OS task queues) under various scheduling policies | C++

Unified Designs for High Performance LDPC Decoding on GPGPU
Boosted decoding by 131X on a GTX 470 vs. a Westmere Xeon CPU | CUDA

Developing a Linux-Like Kernel from Scratch
Implemented interrupt initialization, paging, context switches, scheduling, and a shell program | C and x86 assembly

SKILLS

Programming
C, C++, Python, CUDA, OpenCL, MPI, OpenMP

OS / Hypervisor
Linux, VMware ESXi

ISA
x86, RISC-V

Compiler
LLVM, JIT compilation (Pin)

Architecture Simulation
ZSim, gem5, GPGPU-Sim, SST

Hardware Design
SystemVerilog, Chisel, Synopsys ASIC toolchain

Software Testing
pytest, Jenkins

Relevant Coursework
Advanced Computer Arch.
Advanced Compilers
Advanced Programming Tools
Computer System Analysis
Data Centers
High-Speed Arithmetic
Machine Learning

AWARDS

Graduate Fellowship
UT Austin Cockrell School of Engineering, 2015-2019

Exchange Student Scholarship
NCTU and UIUC, 2013

Six-Time Winner of Academic Achievement Award (top 3 in class)
NCTU, 2010-2013

†https://lph.ece.utexas.edu/users/hamartia/

PUBLICATIONS

Conference Papers

C. Chang, W. Yin, M. Erez, "Assessing The Impact of Timing Errors on HPC Applications," In Proceedings of The International Conference for High Performance Computing, Networking, Storage, and Analysis (SC). Denver, CO. November, 2019.

C. Chang, S. Lym, N. Kelly, M. B. Sullivan, M. Erez, "Evaluating and Accelerating High-Fidelity Error Injection for HPC," In Proceedings of The International Conference for High Performance Computing, Networking, Storage, and Analysis (SC). Dallas, TX. November, 2018.

O. Subasi, **C. Chang**, M. Erez, S. Krishnamoorthy, "Characterizing the Impact of Soft Errors Affecting Floating-point ALUs using RTL-level Fault Injection," In Proceedings of the 47th International Conference on Parallel Processing (ICPP). Eugene, OR. August, 2018.

S. Lym, H. Ha, Y. Kwon, **C. Chang**, J. Kim, M. Erez, "ERUCA: Efficient DRAM Resource Utilization and Resource Conflict Avoidance for Memory System Parallelism," In Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA). Vienna, Austria. February, 2018.

Journal Articles

B. C. Lai, C. Y. Lee, T. H. Chiu, H. K. Kuo, **C. K. Chang**, "Unified Designs for High Performance LDPC Decoding on GPGPU," In IEEE Transactions on Computers (TC), vol.PP, no.99, 2016.

Workshop Papers

C. Chang, G. Li, M. Erez, "Evaluating Compiler IR-Level Selective Instruction Duplication with Realistic Hardware Error," Workshop on Fault Tolerance for HPC at eXtreme Scale (FTXS). Denver, CO. November, 2019

C. Chang, M. Erez, "A High-Fidelity, Low-Overhead and Open-Source Timing Error Injector," Workshop on Silicon Errors in Logic–System Effects (SELSE). Palo Alto, CA. March, 2019.

C. Chang, S. Lym, N. Kelly, M. B. Sullivan, M. Erez, "Hamartia: A Fast and Accurate Error Injection Framework," Workshop on Silicon Errors in Logic–System Effects (SELSE). Boston, MA. April, 2018. **Best of SELSE** (invited to present at DSN 2018)

H. Menon, **C. Chang**, K. Mohror and M. Erez, "Identifying Critical Variables Using Algorithmic Differentiation for a Realistic Fault Model," Workshop on Silicon Errors in Logic–System Effects (SELSE). Boston, MA. April, 2018.